UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,043	04/18/2001	Gary Dan Dotson	01AB028	9193

7590 08/20/2004

Alexander M. Gerasimow
Rockwell Automation (Allen-Bradley Co., Inc.)
1201 South Second Street
Milwaukee, WI 53204

EXAMINER	
CHAUHAN, ULKA J	

ART UNIT	PAPER NUMBER
2676	13

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/837,043	DOTSON, GARY DAN	
	Examiner	Art Unit	
	Ulka J. Chauhan	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,9,17-20,22,23,25-28 and 30* is/are rejected.

7)☒ Claim(s) *7,10-16,21,24 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 8, 9, 17-20, 22, 23, 25-28, and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,900,886 to Shay.

4. As per claim 1, Shay discloses a video controller raster engine… comprising:

a first in first out (FIFO) memory that interfaces a host bus in the computer system with the raster engine and obtains video data from the frame buffer via the host bus to provide video data to a video pipeline (c. 4 ll. 22-45*: Graphics data for the display controller 30 is stored in an external system memory 31, a DMA controller 35 transfers the graphics data from the external system memory 31 to the display controller 30, and the display controller 30 converts the graphics data into display data and sends the data to the display*; c. 8 ll. 59-c. 9 ll. 17 and Figs. 9 and 15A*: the display controller 30 includes a FIFO memory core 90 and the display controller 30 uses DMA transfers to transfer graphics data 42 from the external system memory 31 to the FIFO memory core 90;* Fig. 1: *the display controller interfaces with the host bus through the DMA controller 35 and the bus interface unit 47*);

a first input counter that has a first input counter value indicative of video data obtained from the frame buffer (Fig. 15A: *write address counter within FIFO write control 98*);

a first output counter that has a first output counter value indicative of video data provided to the video pipeline (Fig. 15A: *read address counter 106*); and

a control logic system, associated with the FIFO memory, that provides an underflow indication according to the first input and output counter values (Fig. 15A and c. 13 ll. 35-62: *the quantity of graphics data stored in the FIFO memory core 90 is monitored as it decreases; The difference between the read address and the write address is computed by the FIFO write control block 98, and when the difference falls below the FIFO threshold level, a FIFO read/write difference count signal rw_diffcnt is generated. The DMA interface control block 84 generates a data request signal DRQ in response to the read/write difference count signal rw_diffcnt in order to initiate the transfer of more graphics data to the FIFO memory core 90.*)

5. As per claim 2, Shay discloses that the underflow indication comprises an underflow signal indicating at least one of an existing underflow condition, an anticipated underflow condition, and a raster engine lockup condition (Fig. 15A and c. 13 ll. 35-62: *The difference between the read address and the write address is computed by the FIFO write control block 98, and when the difference falls below the FIFO threshold level, a FIFO read/write difference count signal rw_diffcnt is generated. The DMA interface control block 84 generates a data request signal DRQ in response to the read/write difference count signal rw_diffcnt in order to initiate the transfer of more graphics data to the FIFO memory core 90*).

6. As per claim 3, Shay discloses that the control logic system provides the underflow signal to a host processor (c. 9 ll. 36-39: *the configuration register block 60 within the display controller includes four configuration registers that control the operation of the display controller 30 and provide status information to an external CPU including FIFO empty interrupt*

and FIFO has run dry; c. 10 ll. 23-27: *configuration register three 66, bits [5:4], FIFTHRS[1:0], set the fraction that the FIFO may empty before a DREQ is generated*; Fig. 12: *FIFO fill thresholds which result from the settings of these bits*).

7. As per claim 4, Shay discloses that the underflow signal indicates one of an existing underflow condition and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other (c. 9 ll. 36-39: *the configuration register block 60 provide status information to an external CPU including FIFO empty interrupt and FIFO has run dry;* Fig. 12 and c. 10 ll. 23-27: *FIFO fill thresholds which result from the settings of configuration register three bits [5:4], FIFTHRS[1:0], indicating the fraction that the FIFO may empty before a DREQ is generated;* c. 13 ll. 35-62: *The DMA interface control block 84 generates a data request signal DRQ in response to the read/write difference count signal rw_diffcnt in order to initiate the transfer of more graphics data to the FIFO memory core 90*).

8. As per claim 5, Shay discloses that the raster engine comprises an underflow threshold value register programmable by a host processor in the computer system, and wherein the control logic system obtains the threshold value from the threshold value register, and compares the threshold value with the difference between the first input and output counter values (c. 9 ll. 36-39: *the configuration register block 60 within the display controller includes four configuration registers that control the operation of the display controller 30 and provide status information to an external CPU;* Fig. 12 and c. 10 ll. 23-27: *FIFO fill thresholds which result from the settings of configuration register three bits [5:4], FIFTHRS[1:0], indicating the fraction that the FIFO may empty before a DREQ is generated;* Fig. 15A and c. 13 ll. 35-62: *The difference between the read address and the write address is computed by the FIFO write control block 98, and when*

the difference falls below the FIFO threshold level, a FIFO read/write difference count signal rw_diffcnt is generated).

9. As per claim 6, Shay discloses that the underflow signal indicates an existing underflow condition when the first input and output counter values are equal, and an anticipated underflow condition when the first input and output counter values are within a threshold value of each other (Fig. 15A and c. 13 ll. 35-62: *The difference between the read address and the write address is computed by the FIFO write control block 98, and when the difference falls below the FIFO threshold level, a FIFO read/write difference count signal rw_diffcnt is generated*; c. 9 ll. 66-c. 10 ll. 1: *Bit [3], FERR, is a FIFO interrupt status bit. A "1" indicates that the FIFO has run dry.*)

10. As per claims 8 and 9, Shay discloses subtracting the first output counter value from the first input counter value to obtain a difference value and providing an underflow indication if the comparison is less than or equal to a threshold value (Fig. 15A and c. 13 ll. 35-62: *The difference between the read address and the write address is computed by the FIFO write control block 98, and when the difference falls below the FIFO threshold level, a FIFO read/write difference count signal rw_diffcnt is generated*).

11. Claims 17-20, 22, 23, 25-28, and 30 are similar in scope to claims 1, 2, 4, and 6-9, and are rejected under the same rationale.

Allowable Subject Matter

12. Claims 7, 10, 11-16, 21, 24, and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art does not disclose or render obvious the combination of elements recited in the claims. Specifically, the cited prior art fails to disclose or render obvious the following limitations: where the underflow signal indicates an existing underflow condition when the first input and output counter values are equal, or less than or equal to a threshold for at least two host clock cycles as per claims 7, 10, 11, 21, 24, and 29; a second input counter, a second output counter, and a raster engine that selectively performs dual scan operation by providing interleaved first and second video data, where an underflow indication is provided according to the first input and output counters and second input and output counter values as per claim 12.

Response to Arguments

14. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6693641 U.S. Patent No. 6460125 U.S. Patent No. 6249756

U.S. Patent No. 5982397 U.S. Patent No. 5900886 U.S. Patent No. 5850572

U.S. Patent No. 5226012

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ulka J. Chauhan whose telephone number is (703) 305-9651. The examiner can normally be reached on Mon. through Fri., 9:30 a.m. to 4:00 p.m.

17. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (703) 308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

18. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ulka J. Chauhan
Primary Examiner
Art Unit 2676

ujc
August 17, 2004